26. The circuit of claim 25 wherein the bias circuit comprises a resistor.

REMARKS

In the Office action dated July 17, 2002, claims 1 - 26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hilbert (U.S. Patent No. 5,983,082) in view of Ciccarelli et al. (U.S. Patent No. 6,175,279 B1).

By this Amendment, Applicants are amending the specification and claims 1, 4, 7, 8, 10, 11, 13, 16, 17, 19 and 24 to correct several typographical errors. No new matter has been added.

Applicants request reconsideration of the rejection of claims 1 - 26 because the cited references, considered either separately or in combination, do not teach or suggest the claimed inventions. The Office action states that application of "the technique of Ciccarelli et al. to the communications system of Hilbert" renders the claimed inventions obvious. However, Ciccarelli et al. does not disclose or suggest structure that when combined with Hilbert results in the claimed inventions.

Claims 1, 8, 17, 20 and 23 are independent claims. Applicants will discuss the rejection of each independent claim in turn.

Response to Rejection of Claim 1 under 35 U.S.C. 103(a)

Regarding claim 1, the Office action states:

> Hilbert discloses a circuit (Fig. 8), comprising: a logic circuit (420 of Fig. 8) having a power input and a power return; a capacitor (805 or 806 of Fig. 8; col. 11, line 21-col. 12, line 13); a first resistor (814 of Fig. 8) having a first end coupled to the power input and a second end to couple to a power source (col. 12, lines 26-32); and a second resistor (815 of Fig. 8) having a first end coupled to the power return and a

second end to couple to a power source return (col. 12, line 33-col. 13, line 65; col. 14, lines 11-65).

However, Hilbert does not specifically disclose a capacitor coupled across the power input and power return; and a first resistor having a first end coupled to the power input and a second end to couple to a power source.

On the other hand, Ciccarelli et al, from the same field of endeavor, discloses an amplifier having an adjustable current source which can be controlled to provide the requisite level of performance at reduced current consumption. The current source can be designed with active devices which are selected based on the logic of the control signals for ease of interface. The bias current is adjusted to provide the requisite level of performance while reducing power consumption (Figs. 3-5; col. 4, lines 40-67; col. 6, lines 13-col. 8, line 29; col. 9, line 25-col. 10, line 40; Figs. 11A-11B, col. 19, line 15-col. 20, line 65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ciccarelli to the communication system of Hilbert in order to minimize power consumption.

Applicants respectfully disagree. Applying the technique of Ciccarelli et al. to the communication system of Hilbert does not produce the claimed invention.

Neither of these references discloses "a first resistor having a first end coupled to the power input and a second end to couple to a power source; and a second resistor having a first end coupled to the power return and a second end to couple to a power source return."

The resistors 814 and 815 of Hilbert connect to the signal outputs 821 and 826 and to NPN transistors 801 and 802 of the variable phase shift network that receive differential signals 819 and 825. Hilbert column 11, lines 36 - 65.

Ciccarelli et al. does not disclose any resistor structure similar to the claim language quoted above. Hence, even assuming there is motivation to combine Hilbert and Ciccarelli et al. (which there is not) the combination does not provide the claimed invention.

Neither of these references discloses "a capacitor coupled across the power input and power return."

The capacitors 805 and 806 in Hilbert connect to the signal outputs 821 and 826 and to fixed current sources 800 and 807, and to NPN transistors 804 and 803 of the variable phase shift network that receive differential signals 819 and 825. Hilbert column 11, line 36 - column 12, line 13.

The adjustable current source as disclosed in Figures 5A, 5B, 11A and 11B of Ciccarelli et al. include a "capacitor 1598 [that] connects across the output of current source 1580 and analog ground." Again, the combination of Hilbert and Ciccarelli et al. does not provide the claimed invention.

Regarding dependent claims 2-5, the Office action states:

> Hilbert as modified discloses a circuit (Fig. 8), comprising: a logic circuit (420 of Fig. 8) wherein the logic circuit comprises a differential circuit; wherein the two logic gates each comprises an inverter (col. 11, lines 21-66).

Applicants respectfully disagree. Hilbert does not disclose a circuit having a differential circuit with resistors as claimed. Hilbert states at column 14, lines 30 - 37:

> In the preferred embodiment, the variable phase shift network 420 includes the first resistor 814 and the second resistor 815. The resistors 814 and 815 shown in series with r_e in FIG. 8 are optional and help correct for even order distortion that occurs on each emitter with large signal swings. This distortion is not a problem when the in-phase and

quadrature outputs are taken differentially, since even order distortion will then cancel. (Underlining added.)

Hence, resistors 814 and 815 are not used when the inputs and outputs are differential because the resistors are not needed to correct for even order distortion. Thus, Hilbert does not teach or suggest the claimed differential circuit with resistors.

Regarding claims 7 and 16, the Office action states:

> Hilbert as modified discloses a circuit (Fig. 8), comprising: a logic circuit (420 of Fig. 8) wherein the CMOS inverters each comprises a p-channel transistor having a source coupled to the power input, a gate, and a drain, and an n-channel transistor having a source coupled to the power return, a gate coupled to the gate of the p-channel transistor to form an input node, and a drain coupled to the drain of the p-channel transistor to form output node (col. 11, line 21-col. 12, line 32), the differential circuit further having a differential input comprising the input nodes for each of the CMOS inverters, and a differential output comprises the output nodes for each of the CMOS inverters (col. 13, line 3-col. 14, line 60).

Applicants respectfully disagree. Hilbert does not disclose a circuit having "a p-channel transistor having a source coupled to the power input, . . . and an n-channel transistor having a source coupled to the power return, a gate coupled to the gate of the p-channel transistor to form an input node, and a drain coupled to the drain of the p-channel transistor to form an output node" as claimed.

First, Hilbert does not disclose CMOS inverters. Second, the transistors of Hilbert are not connected in the manner claimed. For example, while the bases of Q1 and Q3 may be connected, Q1 and Q3 do

not have "a drain coupled to the drain of the p-channel transistor to form an output node."

In summary, the cited references do not teach or suggest the claimed invention. Accordingly, Applicants submit that independent claim 1 and claims 2 - 7 that depend on claim 1 are allowable.

Response to Rejection of Claim 8 under 35 U.S.C. 103(a)

Regarding claim 8, the Office action states:

> Hilbert discloses a circuit (Fig. 8), comprising: logic means (809 of Fig. 8) for performing a logic function (col. 11, line 21-col. 12, line 13); charge means (805 or 806 of Fig. 8) for storing a charge across the logic means; and isolation means (814 of Fig. 8; col. 12, line 33-col. 13, line 65; col. 14, lines 11-65).
>
> However, Hilbert does not specifically disclose an isolation means for isolating the charging means from a power source.
>
> On the other hand, Ciccarelli et al, from the same field of endeavor, discloses an amplifier having an adjustable current source which can be controlled to provide the requisite level of performance at reduced current consumption. The current source can be designed with active devices which are selected based on the logic of the control signals for ease of interface. The bias current is adjusted to provide the requisite level of performance while reducing power consumption (Figs. 3-5; col. 4, lines 40-67; col. 6, lines 13-col. 8, line 29; col. 9, line 25-col. 10, line 40; Figs. 11A-11B, col. 19, line 15-col. 20, line 65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ciccarelli to the communication system of Hilbert in order to minimize power consumption.

Applicants respectfully disagree. Applying the technique of Ciccarelli et al. to the communication system of Hilbert does not produce the claimed invention.

Hilbert does not disclose "charge means for storing a charge across the logic means." Capacitors 805 and 806 in Hilbert connect to the signal outputs 821 and 826 and to fixed current sources 800 and 807, and to NPN transistors 804 and 803 of the variable phase shift network that receive differential signals 819 and 825. Hilbert column 11, line 36 - column 12, line 13. Hence, the capacitors are not across the logic means 809.

Moreover, neither of these references teach or suggest "isolation means for isolating the charging means from a power source." The references do not discuss the need for isolating charging means from a power source, nor do they disclose any structure for doing so.

Regarding claims 9-15, the Office action states:

> Hilbert as modified discloses a circuit (Fig. 8), comprising: a logic circuit (420 of Fig. 8) wherein the charge means comprises a capacitor (805 or 806 of Fig. 8); and the isolation means comprises a first resistor (814 of Fig. 8) to couple a first end of the capacitor to the power source (col. 12, lines 26, 32), a second resistor (815 of Fig. 8) to couple a second end of the capacitor to a return line for the power source (col. 12, line 33-col. 13, line 65; col. 14, lines 11-65).
>
> Claims 11-15 contain similar limitations addressed in claims 2-7, and therefore are rejected under a similar rationale.

Applicants respectfully disagree. Ciccarelli et al. does not contain any language that would suggest configuring the capacitors or resistors of Hilbert in the claimed manner.

In summary, the cited references do not teach or suggest the claimed invention. Accordingly, Applicants submit that independent claim 8 and claims 9 - 16 that depend on claim 8 are allowable.

Response to Rejection of Claim 17 under 35 U.S.C. 103(a)

Regarding claim 17, the Office action states:

> Hilbert discloses a method (Fig. 3 and Fig. 8) of suppressing noise during the switching of a differential circuit having differential inputs and outputs, comprising: charging a capacitor (805 or 806 of Fig. 8) through a resistor (814 of Fig. 8; col. 11, line 21-col. 12, line 13); applying a signal transition at the differential inputs (col. 9, line 22-col. 10, line 66); and circulating charge between the differential outputs (col. 12, lines 26-32); compensating for loss of the charge on the capacitor during the circulation of charge (col. 12, line 33-col. 13, line 65; col. 14, lines 11-65).
>
> However, Hilbert does not specifically disclose the features of circulating charge between the differential outputs through the capacitor; compensating for loss of the charge on the capacitor during the circulation of charge by recharging the capacitor through the resistor.
>
> On the other hand, Ciccarelli et al., from the same field of endeavor, discloses an amplifier having an adjustable current source which can be controlled to provide the requisite level of performance at reduced current consumption. The current source can be designed with active devices which are selected based on the logic of the control signals for ease of interface. The bias current is adjusted to provide the requisite level of performance while reducing power consumption (Figs. 3-5; col. 4,

lines 40-67; col. 6, lines 13-col. 8, line 29; col. 9, line 25-col. 10, line 40; Figs. 11A-11B, col. 19, line 15-col. 20, line 65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ciccarelli to the communication system of Hilbert in order to minimize power consumption.

Applicants respectfully disagree. Applying the technique of Ciccarelli et al. to the communication system of Hilbert does not produce the claimed invention.

Hilbert does not teach or suggest any techniques or structure for accomplishing noise suppression. This subject is never addressed by Hilbert. Hence, there would not have been a motivation to combine the two references.

Moreover, neither of the references address the subject of "circulating charge between the differential outputs through the capacitor." Hence, they do not teach the claimed method.

Regarding claim 19, the Office action states:

> Hilbert as modified discloses a method (Fig. 8) of suppressing noise during the switching of a differential circuit having differential inputs and outputs (col. 9, line 22-col. 10, line 66), comprising clocking the differential circuit after the transition of the signal at the differential output, the circulation of the charge being initiated by clocking the differential circuit, the resistor and capacitor having a time constant that is less than half the clocking frequency (col. 7, line 28-col. 8, line 67).

Neither of the references discusses "circulation of the charge being initiated by clocking the differential circuit" or "resistor and

capacitor having a time constant that is less than half the clocking frequency."

In summary, the cited references do not teach or suggest the claimed invention. Accordingly, Applicants submit that independent claim 17 and claims 18 - 19 that depend on claim 17 are allowable.

Response to Rejection of Claim 20 under 35 U.S.C. 103(a)

Regarding claim 20, the Office action states:

> Hilbert discloses an integrated circuit (Fig. 4 and Fig. 8), comprising: a differential circuit having a power input (col. 6, lines 10-65); the differential circuit further comprises a power return (col. 7, line 28-col. 8, line 67; col. 11, line 21-col. 12, line 13).
>
> However, Hilbert does not specifically disclose an inductor having a first end coupled to the power input and a second end to couple to a power source; and a second inductor having a first end coupled to the power return and a second end to couple to a power source return.
>
> On the other hand, Ciccarelli et al, from the same field of endeavor, discloses an amplifier having an adjustable current source which can be controlled to provide the requisite level of performance at reduced current consumption. The current source can be designed with active devices which are selected based on the logic of the control signals for ease of interface. The bias current is adjusted to provide the requisite level of performance while reducing power consumption (Figs. 3-5; col. 4, lines 40-67; col. 6, lines 13-col. 8, line 29; col. 9, line 25-col. 10, line 40; Figs. 11A-11B, col. 19, line 15-col. 20, line 65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ciccarelli to the communication system of Hilbert in order to minimize power consumption.

Applicants respectfully disagree. Applying the technique of Ciccarelli et al. to the communication system of Hilbert does not produce the claimed invention.

Neither of the references teach or suggest "an inductor . . . coupled to the power input . . . and a power source." Thus, the cited references do not teach or suggest the claimed invention. Accordingly, Applicants submit that independent claim 20 and claims 21 - 22 that depend on claim 20 are allowable.

Response to Rejection of Claim 23 under 35 U.S.C. 103(a)

Regarding claim 23, the Office action states:

> Hilbert discloses a circuit (Fig. 8), comprising: a differential circuit; and a current source (807, 808, 813 of Fig. 8) having an output coupled to the differential circuit; and the current source comprise a transistor (801-804 of Fig. 8) having a drain coupled to the differential circuit, a gate and a source, the capacitor being coupled between the gate and the source (col. 11, line 21-col. 12, line 62; col. 13, line 39-col. 14, line 60).
>
> However, Hilbert does not specifically disclose a current source having an output coupled to the differential circuit, an input, and a capacitor shunting the input.
>
> On the other hand, Ciccarelli et al, from the same field of endeavor, discloses an amplifier having an adjustable current source which can be controlled to provide the requisite level of performance at reduced current consumption. The current source can be designed with active devices which are selected based on the logic of the control signals for ease of interface. The bias current is adjusted to provide the requisite level of performance while reducing power consumption (Figs. 3-5; col. 4, lines 40-67; col. 6, lines 13-col. 8, line 29; col. 9, line 25-col. 10, line 40; Figs. 11A-11B, col. 19, line 15-col. 20, line

65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ciccarelli to the communication system of Hilbert in order to minimize power consumption.

Applicants respectfully disagree. Applying the technique of Ciccarelli et al. to the communication system of Hilbert does not produce the claimed invention.

Neither of the references teach or suggest "a current source having an output coupled to the differential circuit, an input, and a capacitor shunting the input." For example, the current controller 809 of Hilbert and the current sources 1580, 1581 and 1583 do not have "a capacitor shunting the input." Thus, the cited references do not teach or suggest the claimed invention. Accordingly, Applicants submit that independent claim 23 and claims 24 - 26 that depend on claim 23 are allowable.

SUMMARY

In view of the above, Applicants submit that pending claims are in condition for allowance. Accordingly, Applicants request that this application be passed to issue.

Attached hereto is a marked-up version of the changes made to the above-identified application by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

Respectfully submitted,

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By _____

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SDB/dlf

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Page 78, line 17, please amend the paragraph as follows:

FIG. 48a is a block diagram illustrating typical noise coupling paths 2 present on integrated circuit substrate 1 incorporating digital, analog and RF circuitry. A single chip 1 integration of analog 5 digital 6 and radio frequency 3, 4 functions on a single integrated circuit 1 is desirable in applications such as a fully integrated transceiver circuit. In the fully integrated embodiments of the present invention, a silicon substrate 1 includes an integrated transceiver (as shown in Figure 1[~~a~~]) typically incorporating circuit functions 3,4,5,6,7 shown in FIG. 48a. Circuit functions are often classified according to the types of signals present in performing a given function. A transceiver typically processes and generates digital, analog and radio frequency signals. As shown in Figure 48a, radiation and conduction mechanisms 2 tend to create a cross-talk coupling mechanism that allows unwanted signals to be injected at various undesired locations on the integrated circuit 1. It is desirable to utilize a method of integrated circuit construction that tends to eliminate cross-talk and the coupling paths associated with it.

Page 79, line 34, please amend the paragraph as follows:

FIG. 48b is a block diagram of a fully balanced circuit utilizing common mode averaging. A circuit incorporating noise rejection [~~mechanisims~~] mechanisms as shown includes two identical logic gates connected to the power supply V_{DD} and ground through two resistors R1 and R2. In this circuit configuration, a conventionally constructed differential circuit is coupled between a power supply V_{DD} and ground.

Page 82, line 11, please amend the paragraph as follows:

Returning to Figures 48c and 48d of a fully balanced architecture having common mode inductive load, the use of these circuits in

minimizing the sensitivity of analog and RF circuits to spurious noise is described. Circuit inputs and outputs are typically single-ended. Conventionally constructed fully balanced circuits are used in the embodiment of a transceiver shown to avoid the pickup of spurious noise signals. In the embodiment of the invention, having single-ended external connections [~~availible~~] available to an input, output or both, a conventional single-ended to differential circuit is added at each single-ended to differential interface.

Page 82, line 25, please amend the paragraph as follows:

Figure 48e is a block diagram of a [~~full~~] fully balanced architecture having an AC coupled tail current source coupled to ground. Transistor M1 forms a tail current source having its gate AC coupled to ground by capacitor C2. AC coupling the gate to ground eliminates common mode low impedance paths from the ground to the output. Noise is picked up typically through the ground as the ground reference potential varies from noise spikes. Any change in the potential of the ground is transferred to the gate of current source M1. Coupling the gate and source of M1 causes their potential to track each other, tending to prevent the transmission of noise through common mode noise pickup from the ground. Common mode signal rejection is important since common mode signals injected into the differential circuit tend to mix with other differential signals in non-linear devices typically present in the differential circuit. The mixing generates end-band differential spurious signals that are undesirable.

Page 83, line 7, please amend the paragraph as follows:

The fully balanced [~~diferential~~] differential circuit having an AC coupled tail current source includes a resistor R4 coupled between a voltage source VDD and differential circuit power supply terminal +V. A ground terminal GND of the differential circuit is coupled to

the drain of a field effect (FET) transistor M1. The source of M1 is coupled to ground at node 8. The gate of M1 is coupled to a first terminal of resistor R3 and a first terminal of capacitor C2. A second terminal of capacitor C2 is coupled to ground node 8. A second terminal of resistor R3 is coupled to a conventionally constructed bias generator circuit.

Page 83, line 19, please amend the paragraph as follows:

A fully [~~ballanced~~] balanced differential circuit is conventionally constructed as known by those skilled in the art to achieve a desired circuit function. The input and the circuitry in the differential circuit operate fully differentially having an output that is converted [~~internaly~~] internally inside of the differential circuit into a single-ended output. In alternative embodiments, the output is maintained as a differential signal.

In the Claims:

1. A circuit, comprising:

a logic circuit having a power input and a power return;

a capacitor coupled across the power input and the power return;

a first resistor having a first end coupled to the power input and a second end to couple to a power source; and

a second resistor having a first end coupled to the power return and a second end to couple to a power source return.

4. The circuit of claim 3 wherein the two logic gates are the same type of gate.

7. The circuit of claim 6 wherein the CMOS inverters each comprises a p-channel transistor having a source coupled to the power input, a gate, and a drain, and an n-channel transistor having a source coupled to the power return, a gate coupled to the gate of the p-channel transistor to form an input node, and a drain coupled to the drain of the p-channel transistor to form an output node, the differential circuit further having a differential input comprising the input nodes for each of the CMOS inverters, and a differential output [~~comprises~~] comprising the output nodes for each of the CMOS inverters.

8. A circuit, comprising:

logic means for performing a logic function;

charge means for storing a charge across the logic means; and

isolation means for isolating the [~~charging~~] charge means from a power source.

10. The circuit of claim 9 wherein the isolation means comprises a first resistor to couple a first end of the capacitor to the power source, and a second resistor to couple a second end of the capacitor to a return line for the power source.

11. The circuit of claim 8 wherein the logic means comprises a differential circuit.[~~,~~]

13. The circuit of claim 12 wherein the two logic gates are the same type of gate.

16. The circuit of claim 15 wherein the CMOS inverters each comprises a p-channel transistor having a source coupled to the first end of the capacitor, a gate, and a drain, and an n-channel transistor

having a source coupled to the second end of the capacitor, a gate coupled to the gate of the p-channel transistor to form an input node, and a drain coupled to the drain of the p-channel transistor to form an output node, the differential circuit further having a differential input comprising the input nodes for each of the CMOS inverters, and a differential output [~~comprises~~] comprising the output nodes for each of the CMOS inverters.

17. A method of suppressing noise during the switching of a differential circuit having differential inputs and differential outputs, comprising:

charging a capacitor through a resistor;

applying a signal transition at the differential inputs; and

circulating charge between the differential outputs through the capacitor.

19. The method of claim 18 further comprising clocking the differential circuit after [~~the~~] a transition of the signal at the differential output, the circulation of the charge being initiated by clocking the differential circuit, the resistor and capacitor having a time constant that is less than half the clocking frequency.

24. The circuit of claim [~~24~~] 23 wherein the current source comprises a transistor having a drain coupled to the differential circuit, a gate and a source, the capacitor being coupled between the gate and the source.